Pattern Delineation of Deep Trench Arrays on Polished Silicon Surfaces Employing Contrast-photoresists Lithography

Deep Trench Patterning

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Abstract

A delineation process for micrometer size lateral patterns of negative photoresist, on polished silicon surfaces carrying vertical trenches of V-shape and depth in the range of 100-200 micrometers, has been developed by integrating a compatible positive photoresist (S1813) lithography employing single photo mask. Arrays of V-groove patterns of 150 micrometer depth have been delineated with HNR120 photoresist on (100) silicon surfaces for further selective electroplating of metals. The optimized process is compatible with conventional IC process and is cost effective in realizing V-groove inductors for high frequency applications.

Keywords

Photolithography; Deep Trench Pattern; Microelectronics; MEMS; Micro-Inductor

Introduction

Advancement in Micro-Electro-Mechanical System (MEMS) technology and its further integration with microelectronics have paved way into realizing 3-Dimensional micro-structures for new generation of electronic devices (Peter et-al, 2002; Divakaruni et-al, 2001; Hong-Wei et-al, 2001; Zhao et-al, 2009). Integration of inductive components with conventional monolithic electronic circuits has become viable by employing V-groove inductor technology, consisting of nano-composites of soft magnetic materials. V-groove inductor technology leads to reduced circuit size, higher frequency and temperature operations (Dhagat et-al, 2004). With the increasing importance of 3-dimensional micro-structures, non planar surface of silicon wafer owing to presence of V-grooves, restricts the conventional lithographic processes. Thin photoresists with 1-2 micrometer of depth of focus can not be used to delineate deep V-grooves alongside sub-micrometer lateral size patterns. While handling of V-groove of depths in the range of tens to hundreds micrometers, a single photoresist process therefore ceases to delineate sub-micrometer lateral patterns. The batch fabrication process of such patterns further results in distributed 3-Dimensional structures on the entire silicon wafer thus making the pattern delineation be a challenging task while maintaining the yield and the cost.

A number of lithographic processes have been developed to delineate sub-micrometer lateral patterns with deep trenches for various applications. Hybrid lithography (Steen et-al, 2006), contour lithography (Mita et-al, 2006), multi-level exposing (Sharma et-al 2003), suitable baking (Wada et-al, 2004) and employing negative dry film resist [Moon-Youn et-al, 2004] are recently developed techniques to delineate 3-D microstructures with deep trenches. The proposed process differs from the reported techniques in the way of low cost, Integrated Circuit (IC) process compatibility and no extra major process step. The process deals with an optimized combination of conventional negative and positive photoresist systems.

Experimental methodology adopted in this work is explained in the next section by considering a V-groove of 150 micrometer depth in (100) silicon

substrate. A clean pattern of the V-groove masked with negative resist (Hunt Negative Resist) HNR120 has been shown followed by selective electroplating of silver and copper separately. An optimized process is presented with relevant experimental details.

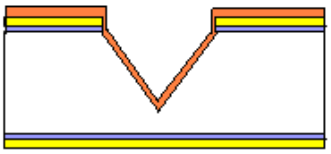
Experimental Methodology

In the process of photolithography, while using Positive Photo Resist (PPR) , patterns are developed in alkaline solutions followed by water rinse for fixing. Upon hard baking and subsequent processes, the hard baked photoresist layer is removed in mild heated acetone. In the case of Negative Photo Resist (NPR), developing process involves organic solutions and excludes from water treatment. Upon hard baking NPR layers require recommended removers with substantial heat treatment followed by hot water rinse in more than single iteration. In view of strong reaction of NPR removers, hard baked patterns of PPR cease to remain in NPR removers. Whereas, selective PPR removers, do not attack hard baked NPR patterns. Therefore the sequence of a PPR photolithography followed by NPR photolithography can be utilized to retain finally an NPR pattern with a complete removal of hard baked PPR. The reverse order of combining the contrast photoresists, ceases to sustain as hard baked PPR patterns do not withstand in chemically stronger NPR remover. The first lithography involving PPR, planarize the V-grooved surface. The second lithography provides NPR masking with clear V-grooves.

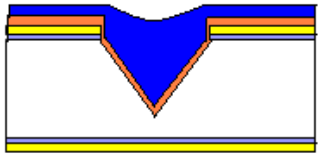
V-groove Patterning Employing Single Photoresist

V-grooves on a polished silicon (100) surface are realized by wet anisotropic etching in alkaline solution such as aqueous Potasium Hydroxide (KOH) with precisely controlled dimensions (Zubel et-al, 1998;1 Bean, 1978). Depth of the cone is 0.7 times of the smallest side of the window pattern. In the case of geometries with dimensions in the range of 100-200 micrometers, depth of the V-grooves lies in the range of 70-150 micrometers. Patterning of such deep V-grooves using photolithography, results in filled V-grooves with photoresist and makes the process incompatible with microelectronic processes. This has been shown in the following;

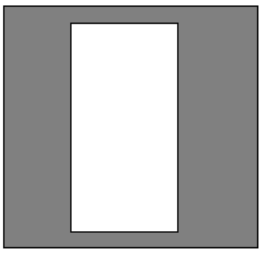
A silicon (100) wafer of 2-inch diameter, equipped with arrays of V-grooves of different lateral dimensions in the range of 50-200 micrometer was considered. After standard device grade cleaning treatment, the silicon wafer was ensured for a complete dry for subsequent photoresist coating. S1813 PPR was coated at 4500 rpm for 30 seconds followed by pre-baking at 90^{o}C for 30 minutes in an oven. This gives the thickness of a PPR layer in the range of 1.1 -1.2 μm (Technical Note, M/s Shipley). A dark field mask of rectangular geometries was employed to expose the PPR coating to delineate the V-grooves. After developing the PPR, V-grooves could not be cleared from PPR due to thickness. The underneath unexposed layer of thick PPR in the V-grooves could not be dissolved in the developer. The schematics shown in Fig. 1 depict the single process with PPR.



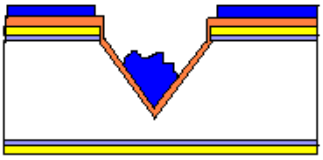
V-GROOVED SILICON(100) WAFER



CROSS SECTION SCHEMATICS AFTER APPLYING PPR COATING



TOP VIEW OF DARK FIELD MASK TO EXPOSE PPR IN V-GROOVE



SCHEMATICS OF PPR TRACES LEFT IN V-GROOVE AFTER DEVELOPING

FIG. 1 SCHEMATICS OF PPR PROCESS FLOW FOR DELINEATING V-GROOVED SILICON WAFER

Patterning of the V-grooves using NPR, bright field

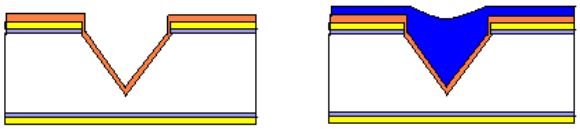
mask is employed. In this case exposed NPR coating remains outside V-grooves, which is retained while unexposed NPR inside the V-grooves is required to be dissolved in the developer. However owing to thicker NPR inside the V-groove, a clear dissolution takes longer time, which results in stripping of exposed NPR pattern. From compatibility point of views, PPR photolithography is preferred over NPR photolithography. However patterning using NPR on planar surfaces (without deep trenches) poses no problem (Technical Bulletin, M/s Olin Hunt). In order to utilize the special characteristics of NPR and PPR, a proper combination of the two photoresists can provide a solution to delineate deep trenches for device applications.

V-groove Patterning Employing Contrast Photoresists

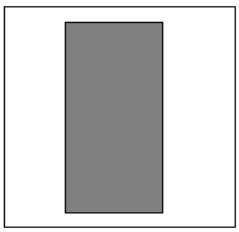
The UV light exposed PPR, becomes dissoluble in its developer while NPR becomes more resistive to its developer. When the deep trenches carrying silicon wafer are first coated with PPR and a bright field mask is employed for photolithography, a trench filled with PPR silicon planar surface is resulted.Upon hard baking of the PPR patterns, the silicon wafer is taken up for NPR coating. At this stage NPR meets with PPR filled trenches and therefore a normal NPR thickness is coated over the entire silicon wafer (Technical Bulletin, M/s Olin Hunt). Again the same bright field mask when used for photolithography, thin NPR layers over the PPR filled in deep trenches (V-grooves) are dissolved in the recommended developer without deteriorating the NPR patterns on the entire silicon wafer. Upon subsequent hard baking of NPR patterns, PPR filled in the trenches is removed in PPR remover which does not reacts with NPR patterns. This way a clear deep trench patterns in NPR environment is obtained for further processing. The schematics of the above stated process flow is shown in Fig.2.

RESULTS AND DISCUSSION

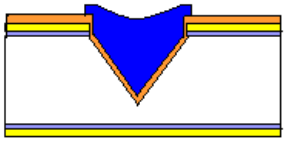
In the fabrication of single loop inductors, V-grooves are realized on the polished surface of 2″ diameter (100) silicon, employing anisotropic etching in aqueous KOH or Tetra Methyl Ammonium Hydroxide (TMAH) at 70 – 80°C. A composite layer of thermally grown SiO_2 of 0.5 μm thickness and LPCVD silicon nitride (Si_3N_4) of 0.15 μm thickness are used as mask for selectivity in the case of etching in KOH, while 1.0 μm thick SiO_2 can work as a mask in TMAH . Each unit of V-grooves of four different dimensions varying between 50-200 μm was arrayed on the entire silicon



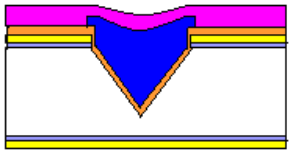
(a)V-GROOVED SILICON(100) WAFER, (b) SCHEMATICS OF V-GROOVE SURFACE AFTER APPLYING PPR COATING



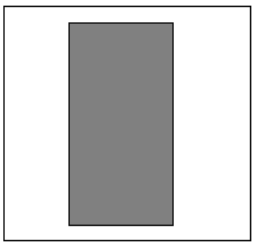
BRIGHT FIELD MASK EMPLOYED TO EXPOSE PPR COATING



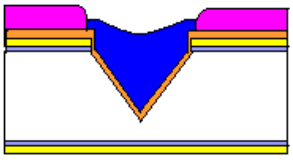
SCHEMATICS OF PLANAR SILICON SURFACE WITH RETAINED PPR IN V-GROOVE



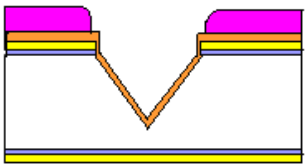
SCHEMATICS AFTER APPLYING NPR COATING



BRIGHT FIELD MASK EMPLOYED TO EXPOSE NPR COATING



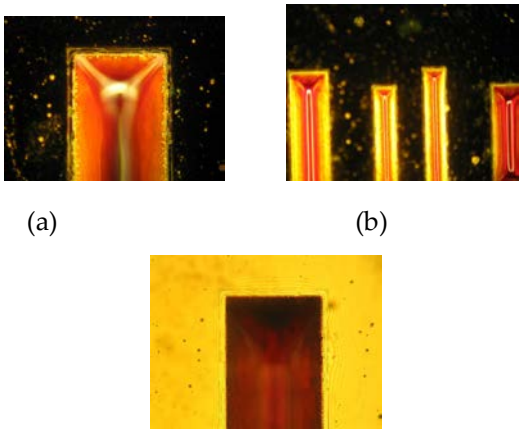
SCHEMATICS OF NPR DEVELOPING WITH EMBEDDED PPR FILLED V-GROOVE



V-GROOVE PATTERN AFTER PPR REMOVAL

FIG. 2 SCHEMATICS OF CONTRAST PHOTORESIST PHOTOLITHOGRAPHY PROCESS FLOW TO DELINEATE V-GROOVE ON SILICON WAFER

wafer. The conventional photoresists of positive and negative tone have been considered for a coating thickness in the range of 1.0 μm. After drying silicon wafers with V-groove array, a coating of PPR S1813 from M/s Shipley was done on one batch of the wafers (Technical Note, M/s Shipley) in order to show the limitations of using single photoresist lithography for delineation of deep trenches. Dark filed of mask was used to delineate V-groove using PPR S1813. The exposure time was increased from 4.0 sec to 8.0 sec on different samples. In each case remains of PPR in the trench were observed with deteriorating PPR pattern with increasing either developing time or exposure time or combination of both. Fig. 3 shows typical details of PPR remains in the trenches after PPR photolithography.



(a) (b)

(c)

FIG.3 OPTICALVIEW OF PPR PHOTOLITHO-GRAPHY; (a) DARK OPTICAL VIEW OF REMAINING PPR IN THE CAVITY, (b) FOUR SIZES OF DEEP V-GROOVES PATTERNED USING PPR, (c) BRIGHT OPTICAL VIEW OF PPR PATTERNED V-GROOVE WITH REMAINING PPR IN THE CAVITY

On the second batch of V-grooved silicon wafers, PPR coating was done and a bright field mask of the same pattern was used to remove PPR from outer area of V-groove using lithography process. A PPR filled V-grooves are resulted. After post baking the PPR patterns, a coating of NPR HNR120 from M/s Waycoat was carried out (Technical Bulletin, M/s Olin Hunt) which is followed by pre-baking, subsequently exposure was done after alignement with the same bright field mask. The NPR layer coating outside V-grooves becomes hard and V-grooves remains filled with hard baked PPR layers. After hard baking of the resulting NPR pattern, a treatment of PPR remover S1112A at 70°C strips away PPR layers from V-grooves leaving NPR patterns unaffected with clear V-grooves. Fig. 4 shows typical details of NPR patterns of V-grooves with clean surfaces. The process has been implemented for selective electroplating of silver and copper on the V-grooves in order to show the clarity of the V-groove surfaces. Silver and copper electroplated V-groove pattern has been shown in figure-5. The process recipe has been tabulated in the following with relevant details.

Recipe

PPR – S1813

Spin coating – 4500 rpm – 30 sec

Pre-baking @ 90 °C – 30 min

Exposure – 350 watt Hg Arc UV-lamp/400 nm 4.0 sec

Developer – MF 312 : DI water – 50:50– 1.0 min

Hard baking @ 120 °C – 40 min

NPR – HNR 120

Spin coating – 4500 rpm – 30 sec

Pre-baking @ 90 °C – 30 min

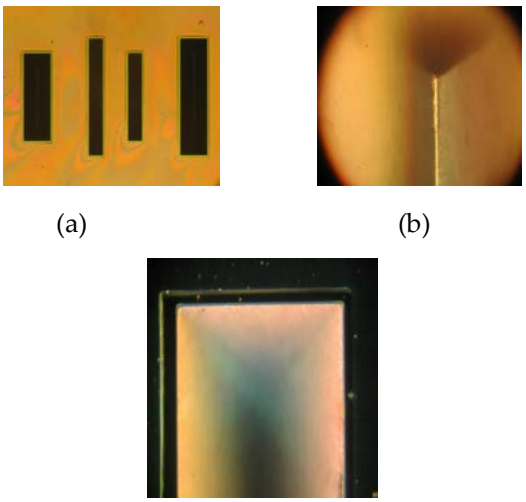
Exposure – 350 watt Hg Arc lamp UV-lamp/400 nm 4.0 sec

Developer – 1.0 min, Developer + n-butyl acetate – 15 sec

n-butyl acetate – 15 sec

Post baking @ 140 °C – 30 min

PPR remover – S1112A @ 70 °C – 3 min

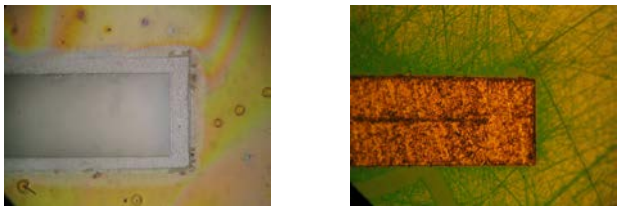


(a) (b)

(c)

FIG. 4 OPTICAL VIEW OF PATTERNS DELINEATED USING CONTRAST PHOTORESIST PHOTOLITHO--GRAPHY; (a) FOUR SIZES OF DEEP V-GROOVES PATTERNS (b) CLOSE DARK VIEW OF V-GROOVE CLEAR DELINEATION, (c) CLOSE DARK VIEW OF NPR PATTERN AROUND THE V-GROOVE BOUNDARY

The developer used in the above recipe is a trademark of respective photoresist manufacturer. For further de-



(a) (b)

FIG. 5 OPTICAL VIEW OF SELECTIVE ELECTROPLATING OF (a) SILVER AND (b) COPPER FOLLOWED BY LAPPING, IN THE V-GROOVE WITH NPR PATTERN DELINEATED EMPLOYING CONTRAST PHOTORESIST PHOTOLITHOGRAPHY

-tails regarding recommended developing processes, relevant technical notes are available (Technical Bulletin, M/s Olin Hunt; Technical Note, M/s Shipley). The photoresists used in this work are widely recommended PR systems for microelectronic processes in IC industry. The thickness of coated PR on the flat surface is constraint with lateral dimensions of the pattern and therefore it has no concern with the depth of the trenches. A PR layer thickness of 1.0 μm has been considered in the entire process. The process has advantages in the development of fabrication process of V-groove inductors for high frequency applications. Selective electroplating of silver and copper shown in Fig. 5 demonstrates the viability of the contrast photoresist lithography for deep trenches delineation. The process has compatibility with conventional IC processes and does not require any high temperature treatment. Use of a single mask for the two photoresist lithographies is an additional advantage.

Conclusions

A combination of conventional positive photoresist and negative photoresist has shown a viable lithography process to delineate deep trenches without involving separate masks. The order from positive to negative photoresist is important, which provides a desired pattern on negative resist. The reverse order is not viable as the negative resist stripper attacks positive resist. The process has advantages in the fabrication of single loop V-groove inductor for high frequency applications.

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Ravi Raj Bhatia was born in Pilani, Rajasthan, India, in 1966. He received ITI certificate in Electronics from the Birla Technical Training Institute Pilani, India, in 1989. Furthermore he has completed his Industrial training in Power Electronics laboratory on "100 Watt Solar Power Inverter" at CSIR-Central Electronics Engineering Research Institute (CSIR-CEERI), Pilani, India, in April, 1990.

In December, 1991, he joined the Sensor and Nano-Technology Group (SNTG), CSIR-CEERI, initially as Technician. During this period he has contributed a major role in the operation and maintenance of Photolithography facility at CSIR-CEERI. He has enthusiastically contributed his novel ideas in lithography process optimization for the development of various devices like Optical Splitter, MEMS Pressure Sensor, MEMS Accelerometer, 4H-SiC Schottky diode detector, RF-MEMS switch, Micro heater, Micro-fluidics devices, and MEMS cantilever and so on. His current research interests include development and optimization of suitable polymer for Nano-electronics device applications. Currently, he holds the position of Senior Technician at SNTG, CSIR-CEERI.

In July 2011, Mr. Bhatia has visited SUSS MicroTec Lithography GmbH, Garching, Germany for one week training on MA-6 double sided mask aligner and Nano-Imprint Lithography (NIL) . He has made numerous technical presentations at CSIR-CEERI and other places and has been co-author of over 15 research papers in refereed scientific journals and conference proceedings.